Design of High Performance Operational Transconductance Amplifier

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***DOI**: https://doi.org/10.34293/acsjse.v3i2.81*

Abstract - *Designing high-performance analog circuits is becoming increasingly challenging with the persistent trend toward reduced supply voltages. The main bottleneck in an analog circuit is the operational amplifier. At large supply voltages, there is a trade off among speed, power, and gain, amongs to ther performance parameters. Often these parameters present contradictory choices for the op-amp architecture. At reduced supply voltages, output swing becomes yet another performance metric to be considered when designing the opamp. Of the several architecture folded cascode OTA is used in which all the transistors are in saturation regime. Furthermore, in an effort to reduce costs and integrate analog and digital circuits onto a single chip, the analog designer must often face the challenges using CMOS processes. This paper covers the design and implementation of a novel CMOS folded cascode OTA designed in 1 m technology. Covered topic include current source and sinks, differential amplifier, compensation techniques, two stage compensated OTA and cascode OTA. Our design emphasis is on practical design where power consumption and speed are critical. The OTA has very low settling time and can be used for high speed applications, such Analog-to–Digital converters, high speed Sigma-delta ADC.*

Keywords: *Operational Trans conductance Amplifier, Analog to Digital Converter, Complementary Metal Oxide Semiconductor. Operational Amplifier, PMOS, NMOS.*

I INTRODUCTION

As the existing need for compact device that could be easily employed in larger designs motivates the demand for mixed mode integrated circuits increases, the design of analog circuits such as operational amplifiers in CMOS technology becomes more critical. One of the most popular sub-circuits used in analog application [7] is an operational amplifier. In a variety of applications, like A/D converters, switched capacitors filters, summers, integrators, differentiators, comparators, op-ampis a basic building block [1]. The design of op-amps continues to poseach all enge as the supply voltage and transistor channel lengths scale down with each generation of CMOS technologies. Op amp is generally defined as a “High gain differential amplifier”. In an opamp driving on-chip devices, output buffer stage can be avoided thus achieving higher speeds and reduction in area and power dissipation. Suchun-buffered opamp s are described as Operational Trans conductance Amplifier (OTA) [5].

The performance parameters of an opamp is characterized by a number of performance measures such as open-loop voltage gain, small signal bandwidth, output swing, linearity, input common mode voltage range, common mode

rejection ratio, slew rate at unity gain, noise and offset and so on[4]. This paper aims at the design of high performance folded cascode OTA using CADENCE Virtuoso tool. The design emphasizes on the major performance parameter like low power, high gain, high CMRR, better UGB, settling time and slew rate.

II CURRENT SINKS, CURRENT SOURCES AND CURRENT MIRRORS

A current sink and current source are two terminal components whose current at any instant of time is independent of the voltage across their terminals [2]. The current of a current sink or source flows from the positive node, through the sink or source, to the negative node.

A. Current Sink

A current sink typically has the negative node at V_{SS} and implementation of a current sink is shown [1]. The gate is taken to whatever voltage is necessary to create the desired value of current. MOS device are not a good current source in non-saturation region [8]. In fact, the voltage across the current sink must be larger than V_{MIN} in order for the current sink to perform properly. From Figure 2.1(a) this means that

$V_{OUT} \geq V_{GG} - V_{TO}$ or $V_{OUT} \geq V_{MIN}$

If the source and bulk are both connected to ground; then the small signal output resistance is given by.

$$r_{out} = \frac{1+\lambda V_{DS}}{\lambda I_D} \cong \frac{1}{\lambda I_D} \quad (2.1)$$

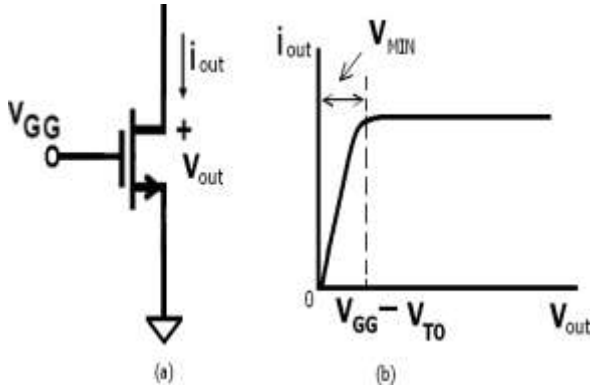

Figure 2.1: (a) Current Sink and (b) Current Voltage Characteristics of Current Sink

B. Current Source

A current source typically has the positive node at V_{DD}. The gate is taken to whatever voltage is necessary to create the desired value of current [1].

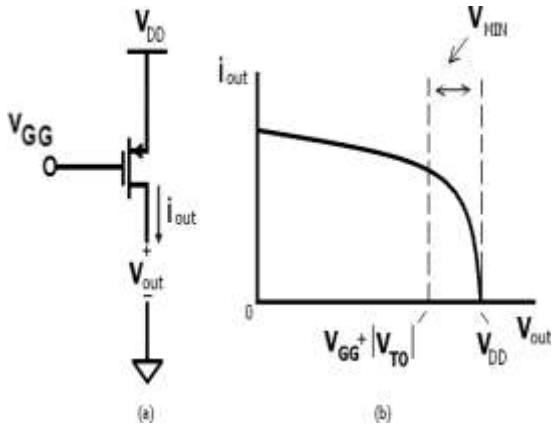

Figure 2.2: (a) Current Source and (b) Current Voltage Characteristics of Current Source

The gate is taken to a constant potential, as is the source. The small signal output resistance is given for current source is by

$$r_{out} = \frac{1+\lambda V_{DS}}{\lambda I_D} \cong \frac{1}{\lambda I_D}$$
$$V_{OUT} \leq V_{GG} + |V_{TO}| \qquad (2.2)$$

The advantage of current sink and sources is their simplicity. However, there are two areas in which their performance may need be improved for certain applications [1].

- Increase the small signal output resistance which results in a more constant current over the range of V_{OUT} values.
- Reduce the value of V_{MIN}, thus al lowing a larger range of V_{OUT} over which the current source/sink works properly.

C. Current Mirrors

Current mirrors are simply an extension of the current sink/source. The current mirror uses the principle that if the gate-source potential softwo identical MOS transistors are equal, the channel current should be equal [1]. In current mirror the current established in one part of the circuit is mirrored at the output. It is used in the biasing of differential amplifier in OPAMP.

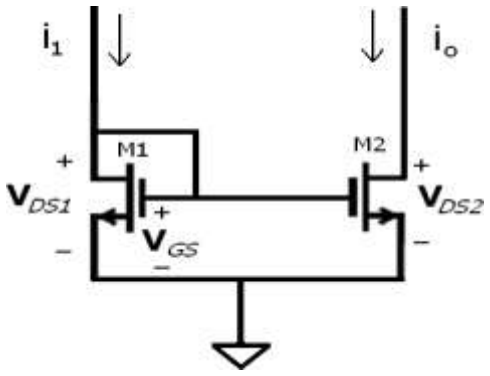

Figure 2.3 Current Mirror

III OTATOPOLOGIES

Primary requirement of an op-amp is to have an open-loop gain that is sufficiently large to implement the negative feed back concept. Most of the amplifiers do not have a large enough gain. Consequently, most CMOS op-amps use two or more stages of gain. Three of the most popular op-amptopologies are

- 2stage
- Cascode
- Folded cascode

The 2 stage op-amp design is simple yetrobust implementation of an op-amp and it can be used as the starting point for the development of other types of op-amps [3]. The folded cascode architecture was developed in part to improve the ICMR and PSSR of the 2 stage op-amp. One of the advantages of folded cascode is that it has push-pull output, i.e., the op-amp can actively sink or source current from the load. Cascading at the output stage results in higher resistance leading to higher gain. 2stage op-amp requires compensation while the latter two are self-compensating topologies.

A. Folded-Cascode Op Amp

The folded- cascode op amp offers self-compensation, good input common-mode range, and the gain of a two-stage opamp [3]. The problem with the differential amplifier is that it is difficult to get the single-ended output voltage without losing half the gain. However, compensation becomes more complex. A better approach is found in the folded topology op-amps, where the signal current is steered in the opposite direction of DC polarity. However, the gain of this configuration is just that of a single stage. A better approach is to use a cascode mirror, which achieves the gain of a two-stage op amp and allows for self-compensation [6].

IV DESIGN AND IMPLEMENTATION OF FOLDED CASCODE OPAMP

A. Design Specifications

Table 1: Specifications of an OTA

Parameter	Specifications
V_{dd}	3v
A_D	≥ 50dB
Settling time	100ns
Settling accuracy	±5%
Output swing	2v(pp)
C_L	10pF
Power dissipation	<3mW

Table 2: Device Parameters

Device Parameter	PMOS	NMOS	Units
λ	0.05	0.04	V^{-1}
k′	50×10^{-6}	110×10^{-6}	AV^{-2}
VT	-0.7	0.7	V

B. Design Steps

The chosen topology is shown in Figure 4.1 Assume the length of the transistor = L = 1μm. Because of this, L and thus the channel length modulation factor, λ, for all transistors are fixed. i.e.$\lambda_n = 0.04$ and $\lambda_p = 0.05$.

Considering that the circuit can be modeled as a first order system. We have from the equation the RC network,

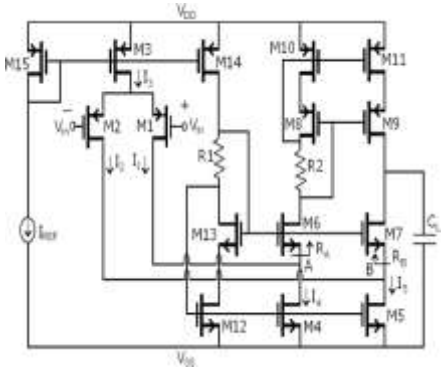

Figure 4.1: A Folded Cascode Op-amp

$$v_{out} = v_{in}\left(1 - e^{-\frac{t}{RC}}\right) \quad (4.1)$$

Att = t_S v_{out} = 0.99v_{in}. Therefore t_S = RCln (100)

$$\Rightarrow RC = 2.17\times10^{-8} \quad (4.2)$$

$$f_{BW} = 1/2\Pi RC = 7.32MHz \quad (4.3)$$

Therefore UGB = 46Mrad/sec. For first order system, slew rate is

$$SR \approx \frac{V_{dd}}{t_s} = \frac{3}{100\times10^{-9}} = 30\times10^{6} \quad (4.4)$$

$$I_3 = SR\times CL = 30\times10^{6}\times10\times10^{-12} = 300\mu A \quad (4.5)$$

Since the values of I_4 and I_5 are normally between I_3 and $2I_3$

$$\therefore I_4 = I_5 \approx 1.1I_3 = 1.1 \times 300 = 330\mu A \quad (4.6)$$

Given that the output voltage swing = 2v⇒ the over drive voltages can be chosen as,

$$V_{ON} \text{ of } M11 + M9 = 0.5V,\ V_{ON} \text{ of } M7 + M5 = 0.5V \quad (4.7)$$

$$\therefore V_{ON} \text{ of } M11 = M9 = M7 = M5 = 0.25v \quad (4.8)$$

$$\left(\frac{W}{L}\right)_7 = \frac{2\times330\times10^{-6}}{110\times10^{-6}\times0.25^2} = \frac{96}{1} \quad (4.9)$$

$$\left(\frac{W}{L}\right)_7 = \left(\frac{W}{L}\right)_5 = \left(\frac{W}{L}\right)_4 = \left(\frac{W}{L}\right)_6 = \frac{96}{1} \quad (4.10)$$

Summaryofthetransistors sizes

$(W/L)_1,(W/L)_2$	20/1
$(W/L)_7,(W/L)_5,(W/L)_4, (W/L)_6$	96/1
$(W/L)_9,(W/L)_8,(W/L)_{10},(W/L)_{11}$	211.2/1
$(W/L)_3$	192/1
$(W/L)_{14}$	21.1/1
$(W/L)_{15}$	19.2/1
$(W/L)_{12}, (W/L)_{13}$	9.6

V SIMULATION RESULTS

A. *Operating Point*

The Schematic of folded cascade OTA is shown in Figure 5.1 and the Schematic for the calculation of DC operating point is shown in the Figure 5.2.

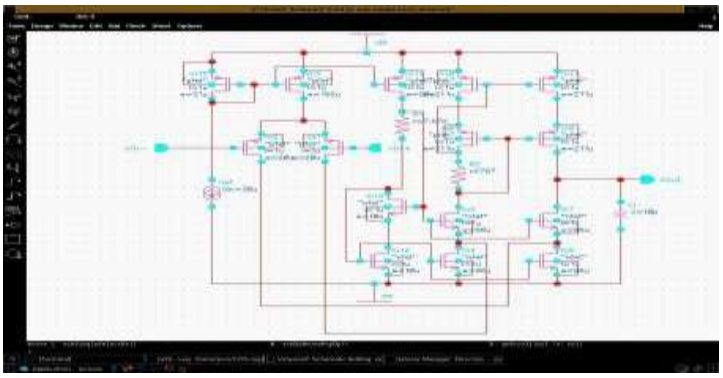

Figure 5.1 Schematic of Folded Cascode OTA

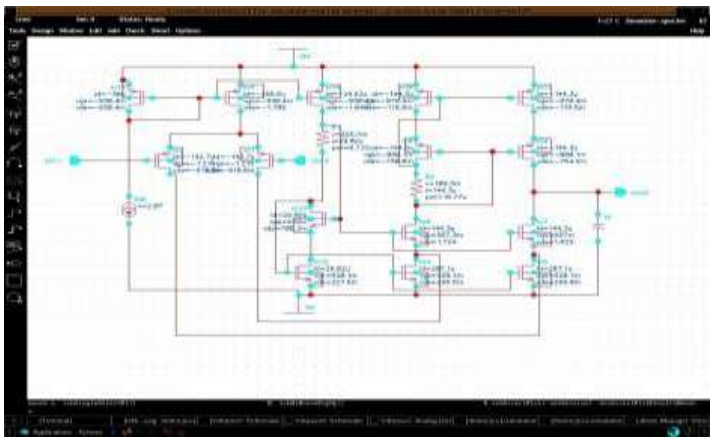

Figure 5.2 DC Analysis

Table 3: Brief Summary of the Operating Points of the Transistors

Transistor	Drain Voltage	Gate Voltage	Source Voltage	Drain Current
M1	1.215	0	296.5m	142.7e-6
M2	1.215	0	296.8m	142.7e-6
M3	1.215	2.07	3	285.5e-6
M4	296.5m	928m	0	287.1e-6
M5	296.8m	928.1m	0	287.1e-6
M6	2.02	296.5m	293.5m	144.3e-6
M7	2.126	1.154	296.8m	144.3e-6
M8	2.13	2.02	2.88	144.3e-6
M9	2.126	2.02	2.88	144.3e-6
M10	2.88	2.13	3	144.3e-6
M11	2.88	2.13	3	144.3e-6
M12	227.9m	928m	0	29.8e-6
M13	928.1m	1.154	227.9m	29.8e-6
M14	1.154	2.07	3	29.8e-6
M15	2.07	2.07	3	30e-6

Table 4: Comparison between Specifications and Simulation Results

Parameter	*Specifications*	*Simulation results*
AVD	≥ 50dB	50.2dB
UGB	7.3MHz	8.895MHz
Settling accuracy	±5%	
Output Swing	2V(pp)	2.28V(pp)
Slew rate(positive)		15.79V/μs
Slew rate (negative)		19.12V/μs
Slew rate (average)		17.455V/μs
Power dissipation	<3mW	1.902mW
AIC		–56.2dB
CMRR		106.4dB

B. Power Dissipation

Power dissipation of folded cascode OTA is given by $P_d = [I_{ref}+I_3+I_{14}+[I_4–I_3/2]2]\ V_{dd} \leq 3mW$

$=30\mu A + 285.5\mu A + 29.82\mu A + [287.1\mu A–285.5\mu A/2]2]V_{dd}$

$=1.902mW.$

C. Ac Respone Magnitude, Ac Response Phase, Transient Response & Commonmode Gain

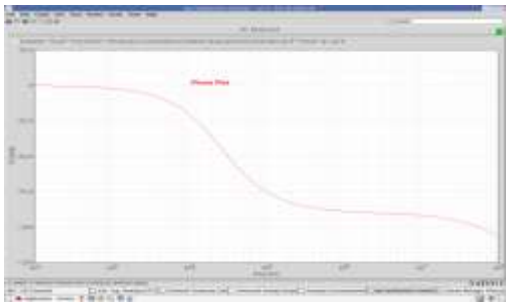

Figure 5.3: AC Magnitude Response

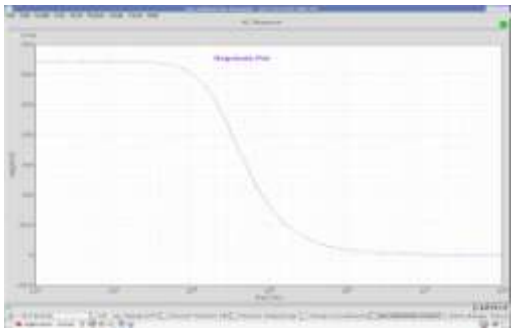

Figure 5.4: AC Phase Response

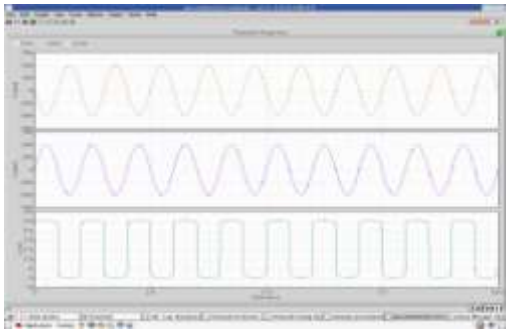

Figure 5.5: Transient Response

CMRR

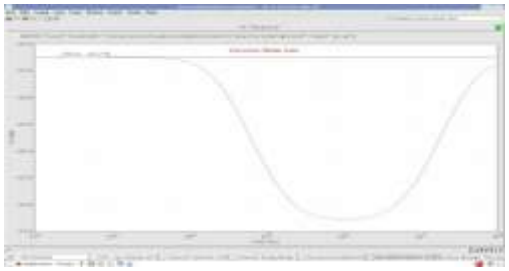

Figure 5.6 Common Mode Gain

$$\frac{A_d}{A_c} = (A_D)_{dB} - (A_C)_{dB} \quad (4.11)$$

= 50.2dB – (–56.2dB)

= 106.4d**B**

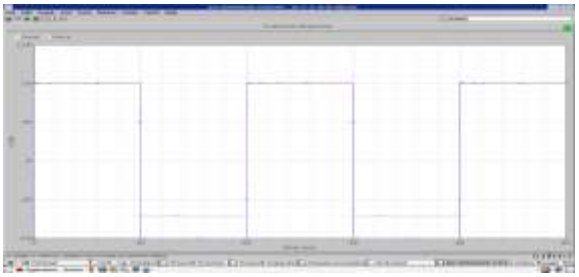

Figure 5.7 Slew Rate Plot

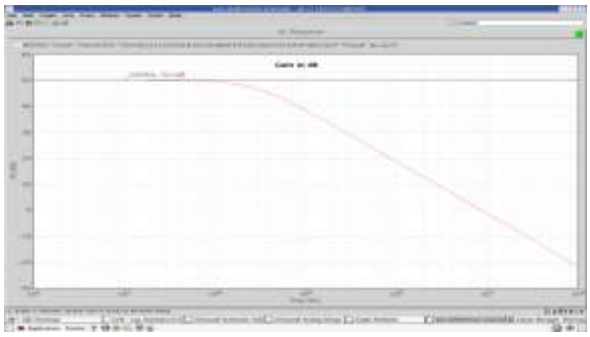

Figure 5.8 Gain Calculation

VI APPLICATION, CONCLUSION AND FUTURE WORK

A. *Applications*

The potential usages of proposed design are

- For simple amplifiers with voltage-controllable gain
- Voltage controlled resistor
- Power System Analog Emulation
- Active filters

B. Conclusion

In the paper folded cascode OTA was designed & simulated successfully, the simulation results confirms the working of OTA. The obtained differential gain, common mode gain, slew rate, & power dissipation met the given specifications. The notable performance areas were the unity gain band width of 8.895MHz & power consumption of 1.902mW. The schematic simulation & analysis were made using CADENCE Virtuoso Analog Design Environment Tool. This OTA consumes less power and has a very low settling time which are the major requirement of modern analog integrated circuits.

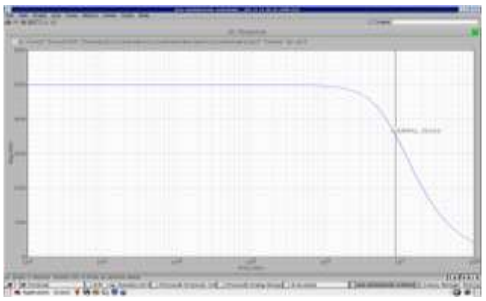

Figure 5.9: UGB Plot & UGB Calculation

Scope for Future Work

Operational Trans Conductance Amplifier (OTAs) have been one of the most significant building blocks in analog signal processors and reconfigurable analog VLSI. Reconfigurability (through controllable gain) is unique feature of OTAs, which is often utilized in filter design. Applications like high frequency continuous time filters requires high trans conductance & good controll ability therefore the OTA is required to have good linearity over its input voltage range for a constant & stable cutoff frequency. Hence in the design process emphasis can be given for providing good controll ability of the OTA. In an analog circuit different active devices should be properly biased to get high performance. Usually a separate bias circuit is used to bias the transistors in an op-amp. The super MOS transistor can be used to construct a folded cascode op-amp to get very high performance. The proposed OTA design can be extended for smaller geometry.

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